REMARKS

The following numbered sections of these remarks are provided in response to similarly numbered sections of the office action.

1. The Examiner has objected to the line spacing of the specification. A substitute specification with double spaced lines is submitted herewith.

2. The Examiner has objected to informalities in claims 1, 7-9, 11-12, 14-17, 19-20 and 26-38 and various claims are amended in response to the objection.

3-13. Claims 1-8, 11, 15-16, 20-27, 30 and 34-35 are rejected under 35 USC 102(a) as being anticipated by US patent 6194928 (HEYNE). Claims 1, 15, 20 and 34 are amended in response to this rejection.

Claim 1

Claim 1 (as amended) recites an apparatus as illustrated, for example, in the applicant's FIG. 1 that produces an output "third pulse sequence" (CLOCK') in response to a first pulse sequence (ROSC) having a period Tp wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period T_P. Claim 2 recites the apparatus comprises:

> first means [first coarse delay circuit 54] for generating … a second pulse sequence [CLOCK] in response to … the first pulse sequence [ROSC], with a first delay adjustable by first control data [SW(A)] with a resolution of Tp/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one
>
> second means [second coarse delay circuit 56] for generating each pulse of the third pulse sequence [CLOCK'] in response to a separate pulse of the second pulse sequence [CLOCK] with a delay adjustable by a second control data [SW(B) with a resolution of T_P/M over a second range substantially wider than T_P/N
>
> a programmable sequencer [58] for changing a magnitude of the first control data [SW(A)] and a magnitude of the second control data [SW(B)] in response to each pulse of the first pulse sequence [ROSC] <u>such that the magnitudes of the first</u>

and second control data vary repetitively in a programmably adjustable manner.

The Examiner points to HEYNE (FIG. 1) as showing two delay circuits connected in series, each with a delay controlled by data (1 and 2) from a control unit (CTR). HEYNE (FIG. 2) shows control unit CTR as being connected in a feedback loop including a phase detector ($\Delta\varphi$). Controller adjusts data 1 and 2 so that the circuit output signal OUT stays in phase with a clock signal CLK. Clearly the feedback control circuit of FIG. 2 is not functionally similar to the recited programmable controller because the control data (1,2) it produces are not repetitive sequences that vary in a programmable adjustable manner as recited in claim 1.

Claim 1 recites that the delay of the first means is adjustable with a resolution of Tp/N and the delay of the second means is adjustable with a resolution of T_p/M, where T_p is the period of the input pulse sequence CLOCK. Nothing in HEYNE suggests that the first and second delay circuits have delay resolutions that are fixed ratios of the period of the input signal IN to the first delay circuit or that they have any relationship to the period of IN. Note from HEYNE FIG. 3 and col. 3, lines 49-54, that the resolution of the first delay circuit is t1, the delay of each inverter I1, and that the resolution of the second delay circuit is t2, the delay of each inverter I2. Thus while HEYNE shows two adjustable delay circuits, they do not have delay resolutions that are integer fractions of the period of an input signal.

HEYNE basically teaches to use two delay circuits to delay a signal, one having a selectable number of gates having a large unit delay per gate and another have a selectable number of gate having a relatively small unit delay per gate. The applicant's invention is an improvement over HEYNE in that it makes the delays of the gate in the first and second delay circuit's integer fractions of the period of the input signal, something that HEYNE does not teach or suggest.

Claim 1 is therefore patentable over HEYNE because HEYNE does not teach or suggest either the recited first or second means having the recited delay resolutions that are integer fractions of the period of their input signal, and does not teach or suggest the recited programmable sequencer for producing repetitive control data sequences

Claim 2

Claim 2 depends on claim 1 and is patentable over HEYNE for similar reasons. Claim 2 further recites, "M and N are relatively prime". As discussed above, nothing anywhere in HEYNE indicates that the inverter delays t1 and t2 which determine the resolution of the two delay circuits are any integer fractions T_p /M and T_p /N of the period T_p of the IN signal. Since the integer ratio factors M and N are not suggested in HEYNE, it is not possible for HEYNE to teach or suggest that M and N are "relatively prime". As explained in the applicant's specification, making M and N relatively prime renders the overall delay resolution of the two circuits together greater than either M or N, a rather surprising result.

Claim 3

Claim 3 depends on claim 1 and is patentable over HEYNE for similar reasons.

Claim 4

Claim 4 depends on claim 1 and is patentable over HEYNE for similar reasons. Claim 4 further recites, "the first range is at least as wide as $(1 - 1/N)T_p$ and the second range is at least as wide as $(1 - 1/M)T_p$. The Examiner indicates that while HEYNE does not directly teach that the second delay unit has a delay as large as T_p one of skill in the art would expect it to have a delay that large. However the Examiner does not indicate that HEYNE teaches or suggests the first delay circuit should have a range is at least as wide as $(1 - 1/N)T_p$. As discussed above, the integer ratio N between delay resolution and input signal period as defined in claim 1 is not taught by HEYNE.

Claim 5

Claim 5 depends on claim 4 and is patentable over HEYNE for similar reasons, and for reasons similar to those discussed above in connection with claim 2.

Claim 6

Claim 6 depends on claim 1 and is patentable over HEYNE for similar reasons.

Claim 7

Claim 7 depends on claim 1 and is patentable over HEYNE for similar reasons. Claim 7 further recites, "the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence, wherein each first gate has a switching delay of T_p/N." As discussed above, nothing in HEYNE suggest that delay t1 of the first delay circuit gates is some integer ratio of the delay of the IN signal. Note in the applicant's FIG. 8 depicting the first delay circuit, that some relatively complicated circuitry is needed to ensure the delay of each gate T_0-T_{N-1} is an integer fraction of the period of the ROSC signal. Compare that to HEYNE's FIG. 1 where there are no provisions for ensuring that the delays of inverters I1 are some integer fraction of the period of the IN signal.

Claim 8

Claim 8 depends on claim 1 and is patentable over HEYNE for similar reasons. Claim 7 further recites, "each second gate has a switching delay of T_p/M". As discussed above, nothing in HEYNE suggest that delay t2 of the second delay circuit gates I2 is some integer ratio of the delay of the IN signal. Note in the applicant's FIG. 8 depicting the first delay circuit, that some relatively complicated circuitry is needed to adjust the delay of each gate T0-TN-1 so that it is an integer fraction of the period of the ROSC signal. Compare that to HEYNE's FIG. 1 where there are no provisions for ensuring that the delays of inverters I1 are some integer fraction of the period of the IN signal.

Claim 11

Claim 11 depends on claim 1 and is patentable over HEYNE for similar reasons. Claim 11 is also distinguishable over HEYNE for reasons set for above in connection with claims 7 and 8.

Claim 15

Claim 15 is patentable over HEYNE for reasons similar to those set forth above in connection with claim 1.

Claim 16

Claim 16 is patentable over HEYNE for reasons similar to those set forth above in connection with claims 1, 7 and 8.

Claims 20, 22, 23 and 25

Claim 20 is patentable over HEYNE for reasons similar to those set forth above in connection with claim 1.

Claims 21 and 24

Claims 21 and 24 are patentable over HEYNE for reasons similar to those set forth above in connection with claims 1 and 2.

Claim 26

Claim 26 is patentable over HEYNE for reasons set forth above in connection with claims 1 and 7.

Claim 27

Claim 27 is patentable over HEYNE for reasons set forth above in connection with claims 1 and 8.

Claims 30, 34 and 35

Claims 30, 34 and 35 are patentable over HEYNE for reasons set forth above in connection with claims 1, 7 and 8.

14-24. Claims 9, 10, 12-14, 17-19, 28, 29, 31-33 and 36-38 are rejected under 35 USC 103(a) as being unpatentable over HEYNE in view of US patent 5471165 (LIEDBERG).

Claim 9

Claim 9 depends on claim 8 and the examiner cites HEYNE as teaching the subject matter of parent claim 8. Claim 9 is patentable over HEYNE for reasons indicted above in connection with claim 8 since the Examiner cites LIEDBERG only as teaching the additional subject matter of defendant claim 9. Claim 9 further recites, "each second and third gate has a similar switching delay of T_p/M set by the magnitude of a second control signal applied to all of the second and third gates". See for example, the applicant's FIG. 7 wherein the control signal CONTROL(B) controls the delay of two sets of gates 60 and 66 so each has a delay of T_p/M, where T_p is the period of the ROSC signal. Gates 66 are merely a part of the delay control mechanism for gates 60, which provide the actual delay of the delay circuit. There are M gates 66 so controller 70 sets the delay of each gate 6 to T_p/M via control signal CONTROL(B). Since gates 60 are similar and receive the same control signal, they provide the same unit delay T_p/M.

The Examiner cites LIEDBERG as teaching the additional limitations of claim 9, as exemplified by the applicant's delay circuit of FIG. 7, but while LIEDBERG's FIG. 1 shows a delay circuit similar to the applicant's FIG. 8 (excluding multiplexer 110), LIEDBERG does not teach a delay circuit having the limitations of claim 9, such as the applicant's FIG. 7, or illustrates the subject matter of claim 9.

Claim 10

Claim 10 depends on claim 9 and is patentable over HEYNE and LIEDBERG for similar reasons.

Claims 12-14

Claims 12-14 depend on claim 11 and are patentable over HEYNE for similar reasons. Claims 12-14 are also patentable over the combination of HEYNE and LIEDBERG for reasons similar to those expressed above in connection with claim 9.

Claims 17-19

Claims 17-19 depend on claim 16 and are patentable over HEYNE for similar reasons. Claims 17-19 are also patentable over the combination of HEYNE and LIEDBERG for reasons similar to those expressed above in connection with claim 9.

Claims 28-38

Claims 28-38 depend on claim 27 and are patentable over HEYNE for similar reasons. Claims 28-38 are also patentable over the combination of HEYNE and LIEDBERG for reasons similar to those expressed above in connection with claim 9.

25. The prior art made of record has been reviewed and does not appear to disclose or suggest the invention as claimed.

In view of the foregoing amendments and remarks it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited as first class mail with the United States Postal Service with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on this 3rd day of June 2004.

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